

In re Patent Application of
ROCHE ET AL.
Serial No. 10/814,823
Filed: MARCH 31, 2004

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The independent claims have been amended to more clearly define the present invention over the cited prior art references. Support for the claim amendments may be found in paragraphs 0045 through 0048, for example. The claim amendments and arguments supporting patentability of the claims are provided below.

I. The Amended Claims

The present invention, as recited in amended independent Claim 1, for example, is directed to a microprocessor comprising a processing unit, and a memory connected to the processing unit and comprising an addressable memory space for a lower memory area and an extended memory area. The microprocessor includes an address bus connecting the processing unit to the memory, and comprising a lower address bus for accessing the lower memory area, and an extended address bus for accessing the extended memory area, and means for executing instructions of an instruction set executable by the processing unit. The instruction set comprises instructions for accessing a first instruction group comprising instructions for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area. The microprocessor also comprises means for forcing to zero an extended address

transmitted by the extended address bus when executing an instruction in the first instruction group so that the lower memory area is accessed.

Independent device Claim 11 has been amended similar to amended independent device Claim 1. Independent method Claim 21 has been amended similar to amended independent device Claim 11.

II. The Claims Are Patentable

The Examiner rejected independent Claims 1, 11, and 21 over Galvin et al. The Galvin et al. reference is directed toward a computer with two operating modes defined by binary data, that is a monitor mode and a user mode. In the user mode, the processor has an access limited to the authorized memory area. In the monitor mode, the processor has an unrestricted access to all the memory. In the user mode, any attempt to access the memory outside the authorized memory area is treated as a fatal error and triggers a trap or exception routine.

Galvin et al. fails to suggest forcing to 0 (zero) an extended part of the access address when an instruction of a first group is executed, as in the claimed invention. In contrast, the microprocessor of Galvin et al. can execute in user mode an instruction which commands access to an unauthorized memory area, which triggers an exception.

In the claimed invention, the criterion for accessing the lower or extended memory area depends on whether the executed instruction belongs to a first or second group of instructions. In contrast, in Galvin et al., the criterion for

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accessing an authorized memory area or outside this area depends on whether the microprocessor is in user mode or the monitor mode. In addition, Galvin et al. discloses privileged instructions executable only in the monitor mode. However these instructions are not disclosed to give access to an extended memory area or outside an authorized memory area, but only as instructions that may or may not cause harm to the computer. Therefore, Galvin et al. fails to disclose a second instruction group distinct from a first instruction group and only comprising all the instructions for accessing an extended memory area.

The Examiner then cited to the 1950 CCPA case of *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) for support that shifting around memory locations of Galvin et al to have monitor code at the "top" of memory is not patentable. *In re Japikse*, which relates to a hydraulic power press, where it was held that there is no invention in shifting a switch that is disclosed by the prior art to a different position since the operation of the device would not be modified.

It is respectfully submitted that the claimed invention is not merely an implementation difference, nor is it a rearrangement of parts, but rather a substantive difference over the prior art. In other words, shifting around the memory locations of Galvin et al. will not result not result in the claimed invention. Moreover, *In re Japikse* applies to moving a mechanical switch in contrast to the claimed invention.

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Applicants further submit that the Examiner is using impermissible hindsight reconstruction based on Applicants' specification as a template to selectively assemble disjoint pieces of the prior art references. Accordingly, it is submitted that amended independent Claim 1 is patentable over Galvin et al. Amended independent Claims 11 and 21 are similar to amended independent Claim 1. Therefore, it is submitted that these claims are also patentable over Galvin et al.


In view of the patentability of amended independent Claims 1, 11 and 21, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

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III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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